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Simple PWM modulator topology with excellent dynamic behavior

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Abstract—This paper proposes a new PWM modulator topology. The modulator is used in switch mode audio power amplifiers, but the topology can be used in a wide range of applications. Due to excellent transient behavior, the modulator is very suited for VRMs or other types of DC-DC or DC-AC applications.

I. INTRODUCTION

Switch mode audio power amplifiers are beginning to show up on market in still greater numbers. Several different modulator topologies, analog or digital, are used together with different control strategies. With the technology of today, analog modulators are superior to digital modulators in terms as linearity, frequency response and dynamic range.

Analog modulators for switch mode amplifiers can be made in a number of ways, but it seems that all the better performing modulators is having the power stage of the amplifier within the control loop, [1, 2, 3, 4, 5] or both power stage and output filter [6].

The proposed topology gives benefits in form of a linear modulator with open loop bandwidth of the switching frequency. This behavior can give benefits in applications other than audio amplifiers, for example in DC-DC supplies with fast transient response. In fact many converters for microprocessors etc. which often requires switching frequencies of 1MHz or higher [7] can be operated with significantly lower switching frequencies without compromising transient behavior, leading to a decrease in switching losses. An example of this will be given later in this paper.

II. BASIC MODULATOR OPERATION

The type most similar to the modulator proposed in this paper is the topology described in [4, 5]:

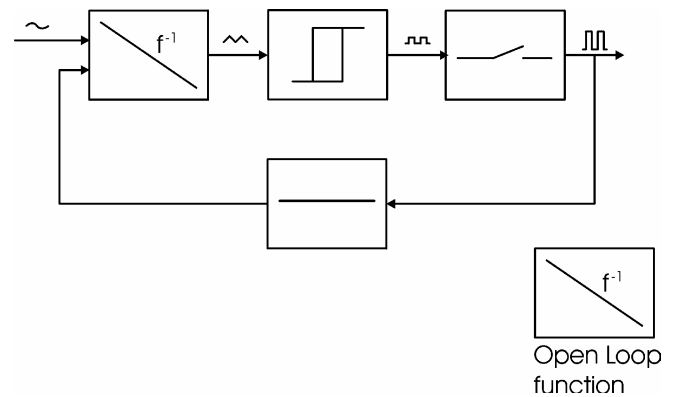


Figure 1 AIM, [4, 5], operation block diagram

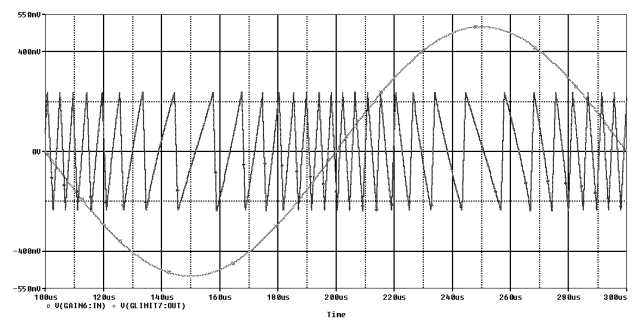


Figure 2 Examples of AIM, [4, 5], reference and carrier signals

The operating principle of the AIM, Astable Integrating Modulator, [4, 5], modulator is hysteresis control of a feedback voltage, which has a lot in common with the hysteresis control with a current feedback signal known from basic switch mode techniques, where the output filter inductor acts as an integrator of the output signal from the power stage.

The feedback signal is the output signal taken from the power stage and is hereby the PWM output signal. An integrator integrates the difference between the output voltage and the reference (audio) signal. If the switching frequency is high compared to the frequency of the input

signal, the input signal can be considered a DC voltage within a single switching period. Following this the integration will be an integration of a square wave signal with positive and negative amplitudes as the difference between the power supply rails and the audio signal. The output from the integrator is hereby a saw tooth signal with positive and negative slopes proportional to the difference between the audio signal and the supply rails. Because of the hysteresis implemented, the saw tooth signal at the output of the integrator is not overlapped with the audio signal.

The AIM modulator benefits from having the power stage included in the modulator loop; hereby errors from the power stage, e.g. dead time distortion and finite slopes of the output voltage as well as errors due to power supply ripple will be suppressed by a factor of the modulator's open loop gain. To introduce further loop gain to the system, and to reduce error related to non linearities of the output filter components, e.g. hysteresis effect of the output inductor core material, the AIM modulator is often combined with additional voltage feedback taken from after the output filter. By combining a modulator including only the output stage with voltage feedback taken after the output filter, stability problems will often occur when the output is either connected to open or light loads due to the very high quality factor of a highly under damped LC filter. To maintain stability under light or open load conditions a RC branch or Zobel network is usual connected from output to ground, giving a minimum load impedance at high frequencies.

The slopes of the carrier signal are related to the actual level of the input signal given by the modulation index, M . $M=0$ is the idle condition, and $M=1$ is the maximum signal level, either positive or negative.

When operating with $M>0$, the integration times for the two slopes of the carrier signal will respectively increase and decrease. Since the decrease is larger than the increase, the actual switching frequency will vary with M :

$$f_s(M) = \frac{1 - M^2}{4\tau_{\text{int}}H + 4t_p}$$

where τ_{int} is the time constant of the integrator, H the ratio between the hysteresis window levels and the power supply rails, and t_p is the propagation delay through the modulator loop.

The idle switching frequency, $f_{s,\text{idle}}$ can be found by setting $M=0$, which leads to:

$$f_s(M) = f_{s,\text{idle}} \cdot (1 - M^2)$$

From this it can be seen that the switching frequency decreases rapidly with M , and actually stops completely for $M=1$. Because of this, it is necessary to limit the maximum modulation index, M , so the switching frequency will be significantly higher than the frequency of the input signal under all operating conditions in order to keep additional control loops within proper operational conditions. Often a maximum of $M=0.8$ is used for this type of modulator.

To avoid the frequency drop at high M to some extent, a variable hysteresis window can be implemented so this window decreases for higher M as proposed in [6]. With this technique, the drop in switching frequency at high M can be significant reduced, and hereby allowing a higher maximum level for M .

The modulator topology proposed in this paper, GLIM – GLocal Integrating Modulator, has the same basic characteristics as the AIM modulator, but operates with feedback signals taken from both the output of the power stage and the output filter. This gives benefits in form of suppression of errors due to power stage and output filter nonlinearities, as well as increasing open load stability and closed loop bandwidth, with or without additional voltage feedback loops.

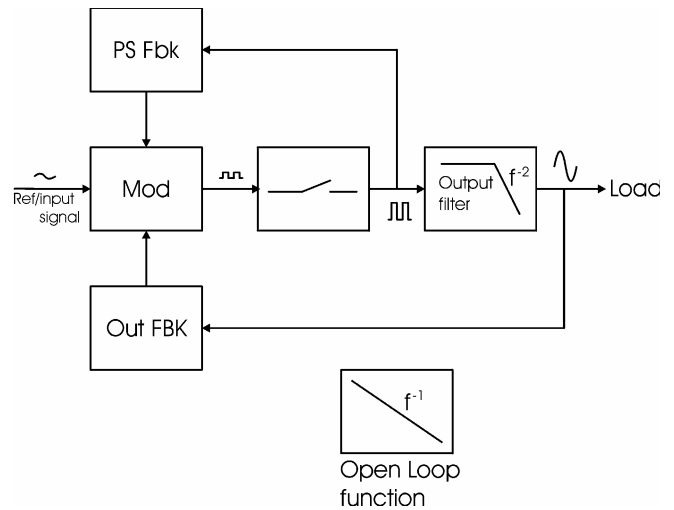


Figure 3 Block diagram of the proposed modulator topology

To obtain the same basic function as the topology shown in Figure 1, the same open loop function for the modulator loop should be obtained. The open loop function should be a pure integrator, which is realized in Figure 4.

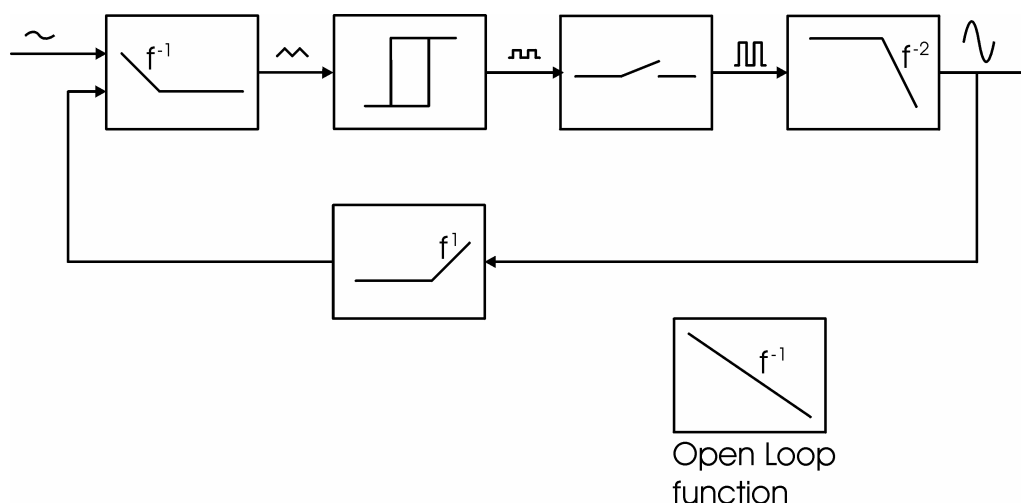


Figure 4 Basic realization of the proposed topology

Since the output filter used is a L-C filter, the combination of the feedback and forward block should have a pole in zero and two zeros at the filter frequency of the output filter. In Figure 4 this is made by a zero in the feedback block at the output filter frequency and a forward block as an integrator with a zero in the filter frequency. Because the output filter is included in the modulator loop, open load stability is obtained because the peaking is directly compensated for in the modulator.

To reduce system complexity, an almost passive model of the modulator loop can be made, using a comparator as the only active component.

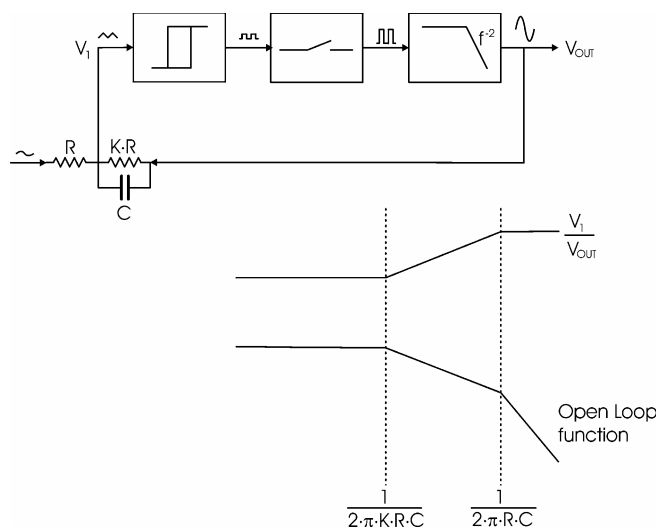


Figure 5 Passive realization of the modulator loop

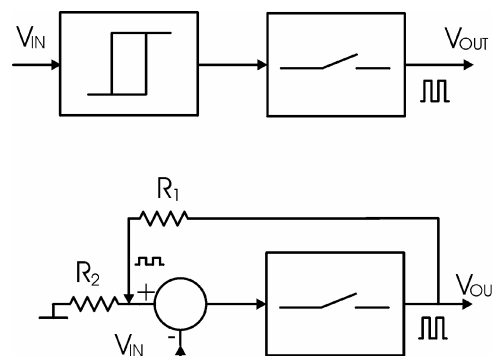


Figure 6 Realization of the schmidttrigger / inner feedback of the modulator loop

In Figure 5 and Figure 6 is shown one way to realize the almost passive modulator loop by combining the feedback block and the forward block into a summing node, V_1 , and realization of the schmidttrigger by using the output level of the power stage as reference for the trigger levels. It is clear that at Figure 5 the open loop function of the modulator loop is no longer a pure integration, but deviates from this by having a constant low frequency gain and a 2. order roll off at high frequencies. This open loop function will compromise performance of the modulator because the carrier signal will no longer be a pure saw-tooth signal, but combining the modulator with one or more extra control loops, these can be designed to compensate for the modulator's deviation from the pure integration as illustrated on Figure 7. Further more the almost passive modulator will not have a high loop gain to reduce errors from especially the power stage, but combined with additional control loop(s) both high resulting loop gain can be obtained as well as high linearity.

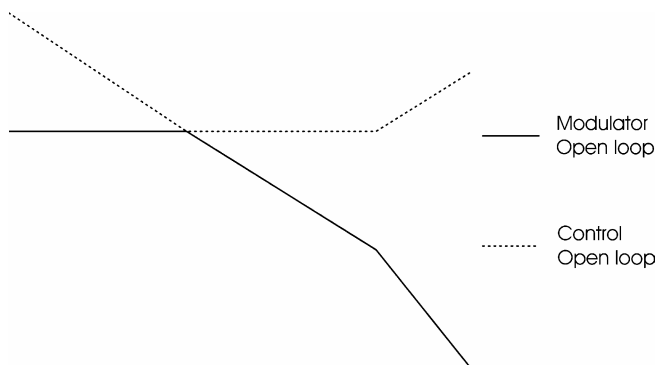


Figure 7 Passive modulator and desired control open loop functions

The definition of the control open loop function in Figure 7 is illustrated for one or more control loops in Figure 9.

The main benefit apart from reduced cost obtained by making the modulator loop almost entirely with passive components is that no operational amplifier in the modulator loop is required. The amount of high frequency signal content from the output of the control loop(s) to make the resulting integrating open loop function is very low, which means that audio performance of the opamps will not be degraded due to non-linearities caused by handling high frequencies at high levels.

III. APPLICATION 1, AUDIO AMPLIFIER, EXPERIMENTAL RESULTS

A single ended prototype power amplifier has been built and tested to verify operation and performance of the proposed modulator topology.

Table 1 Parameters for amplifier prototype

Power supply	+/- 40V
Output power (4Ω load)	125W
Output filter inductor	20uH
Output filter capacitor	352nF
Output filter cutoff (power bandwidth), (ref. to output)	60kHz
Small signal bandwidth (ref. to output)	120kHz
Switching frequency, idle	350kHz
Number of control loops	2
Load impedance	4Ω

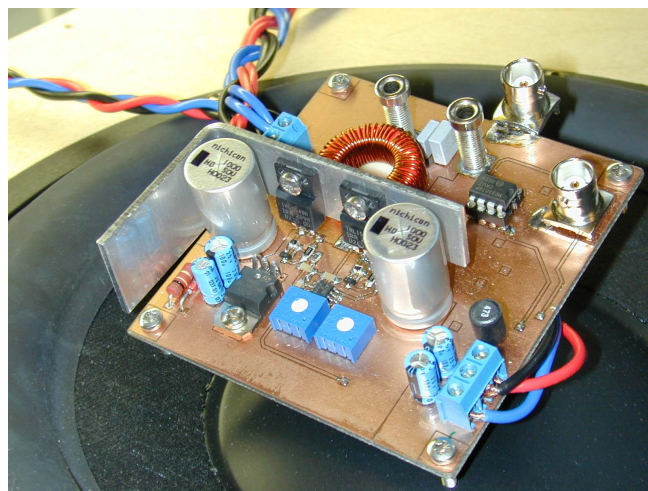


Figure 8 The prototype amplifier

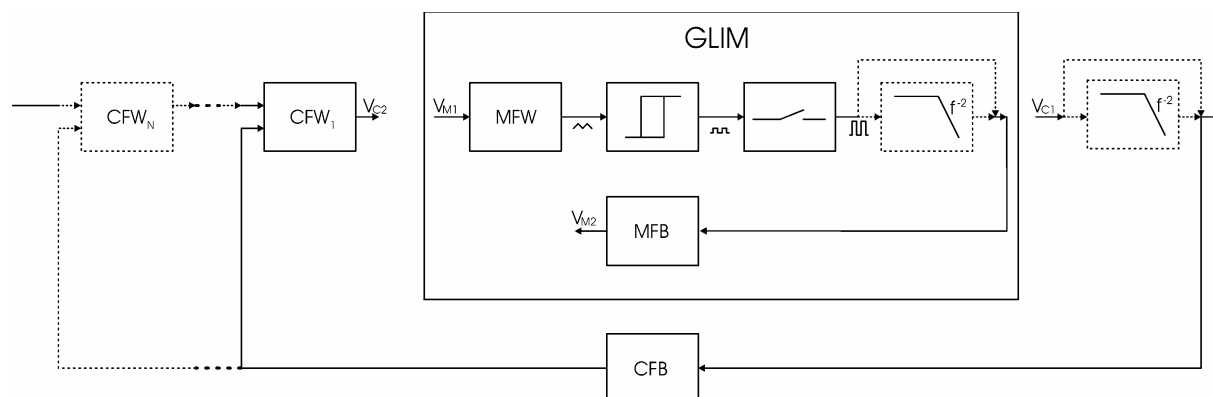


Figure 9 Definition of control open loop function

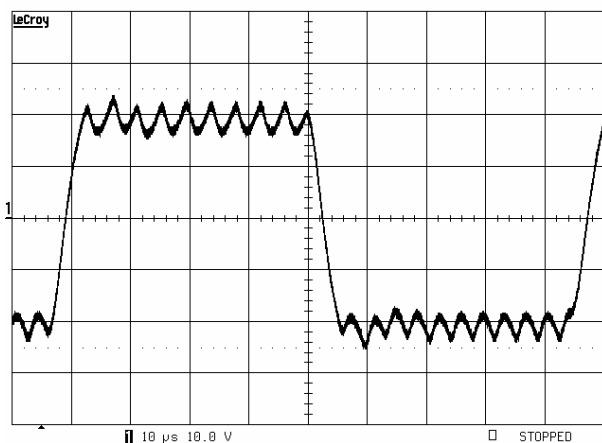


Figure 10 Square output, $M=0.5$, 4W load, $P_{out} = 100W$

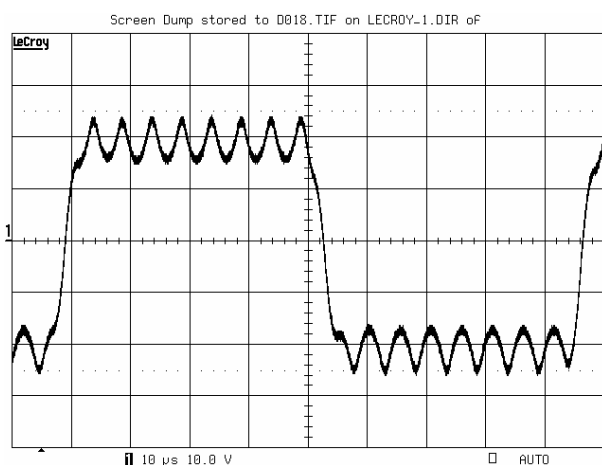


Figure 11 Square output, $M=0.5$, open load

As seen on Figure 10 and Figure 11, the prototype is perfectly stable with normal load conditions as well as with open load.

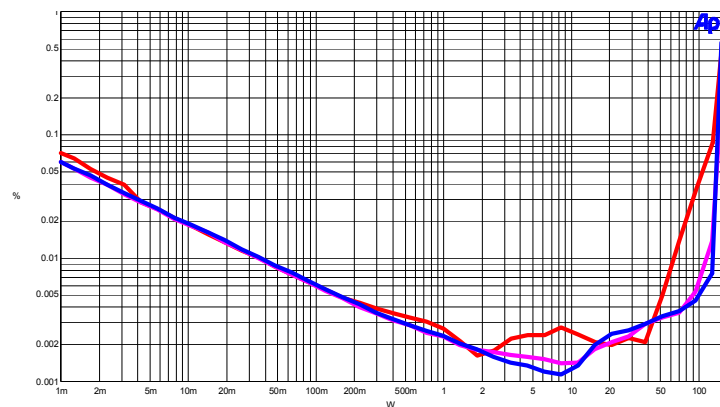


Figure 12 THD+noise vs. output power, from bottom: 100W, 25W, 50W, 100W

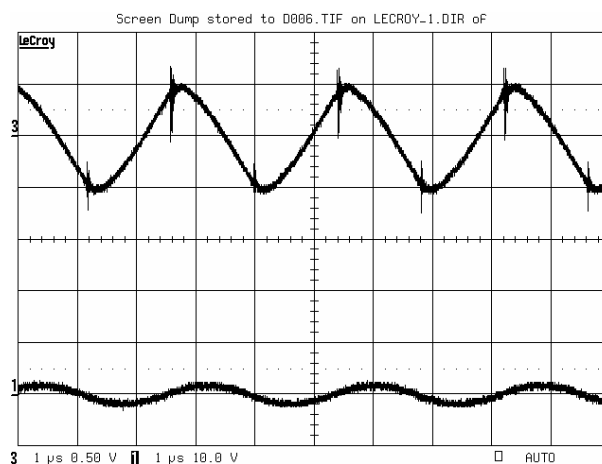


Figure 13 Carrier and output, load 4W, idle

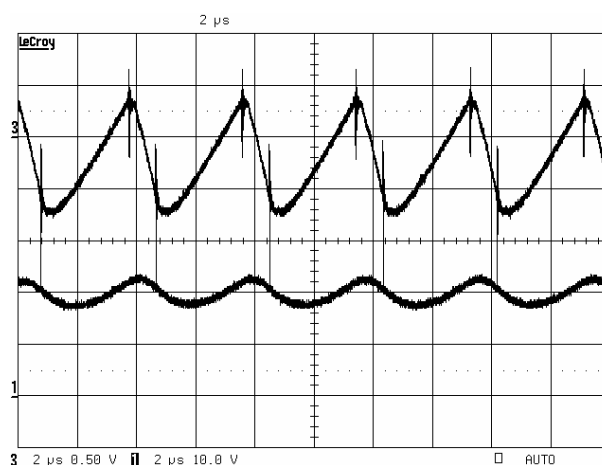


Figure 14 Carrier and output, load 4W, $M=0.5$, $P_{out} = 100W$

Figure 13 and Figure 14 shows carrier signals close to the simulated waveforms. Derivations from the ideal simulations are due to a very low cost implementation.

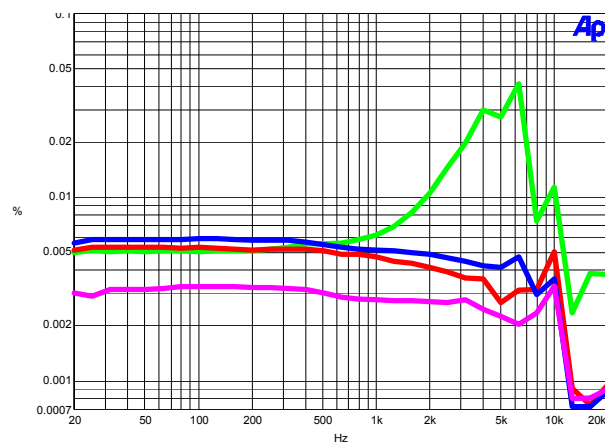


Figure 15 THD+noise vs. frequency, from bottom: 10W, 25W, 50W, 100W

The measurements of THD+noise with (20kHz measurement bandwidth) in Figure 12 and Figure 15 shows outstanding audio performance for both low and high frequencies as well for both small and high output powers. The increase in distortion at higher frequencies at 100W output power is due to the decreased switching frequency and hereby decrease of loop gain and bandwidth.

IV. APPLICATION 2, DC-DC CONVERTER, SIMULATIONS

A DC-DC converter model with the proposed modulator topology has been simulated. The aim of the design is a converter for microprocessor applications, where load step response is of major importance.

Table 2 DC-DC simulation example parameters

Input voltage	5V
Output voltage	3.3V
Output current	30A
Output filter inductor	2.5uH
Output filter capacitor	2000μF
Open loop output impedance	10mΩ
Switching frequency	200kHz
Modulator loop propagation delay	100ns

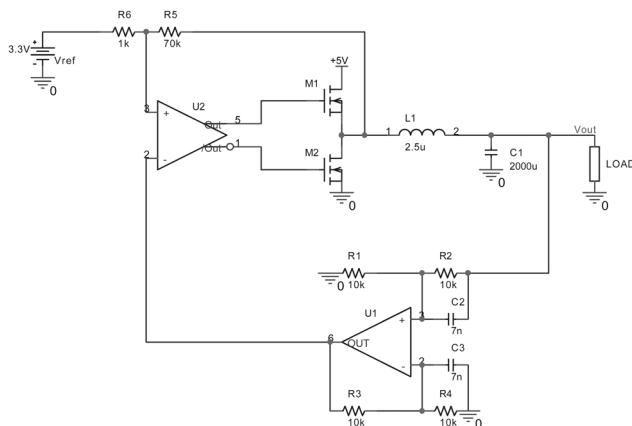


Figure 16 DC-DC converter example schematic

Simulated closed loop DC output impedance of 90μΩ corresponding to a DC loop gain of 41dB using only a single operational amplifier, U1, with an open loop gain of 60dB (37dB with operational amplifier open loop gain of 40dB).

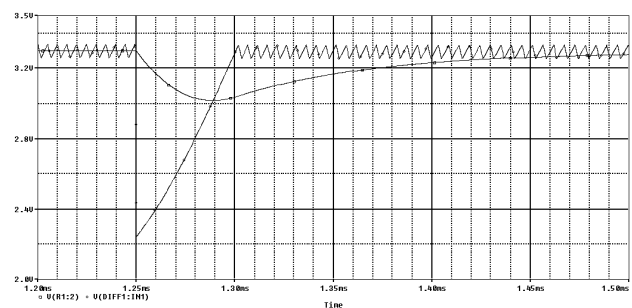


Figure 17 1A-30A load step, output voltage and carrier signal

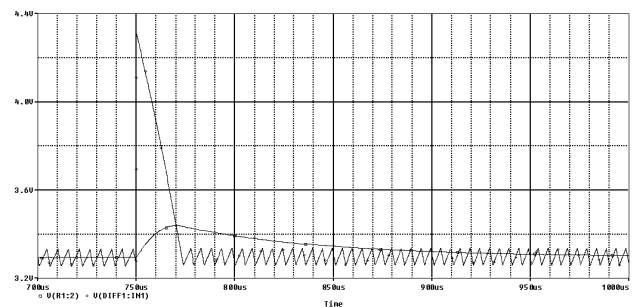


Figure 18 30A-1A load step, output voltage and carrier signal

Time to recover proper operation for the modulator after a 1A-30A load step is 49μs, and 22.5μs for a 30A-1A load step.

ΔU_{out} and settling time for output voltage to 1% is 283mV/146μs for 1A-30A load step and 146mV/118μs for 30A-1A load step.

As well ΔU_{out} and settling time can be further improved by changing output filter component values, and the results should only be seen as an indicator for the very fast response of the modulator.

Often this type of converters is designed with switching frequencies of 1MHz or higher [7] to achieve a desired fast transient response. The usual very high switching frequency is needed to achieve a desired high bandwidth with traditional voltage or current mode control loops, where the switching frequency has to be significantly higher than the loop bandwidth. With the proposed modulator topology the effective loop bandwidth is the same as the switching frequency, and this type of modulators can achieve the same performance at significant lower switching frequencies.

The result shown is only simulations, and no parasitic components have been taken into account. Therefore the simulation results do not show realistic performance as this often will be degraded by especially ESL and ESR of the output capacitor used. What is interesting is the recovery time for the modulator after a significant load step.

For practical fast response DC-DC converters such as VRMs, the proposed modulator topology can either give

same performance as traditional modulators, but at a significant lower switching frequency and thereby with reduced switching losses, or maintain the switching frequency and losses, pushing performance up to an even higher level.

V. CONCLUSION

The proposed modulator topology has been tested in a prototype audio amplifier. The measurements show excellent transient response in both normal and open load working conditions as well as state of the art audio performance, even though the prototype was a very low cost solution.

The simulations of the proposed modulator as a DC-DC converter shows extremely fast recovery after a load step even though the switching frequency is low for the type of application. The modulator topology could be implemented in VRMs or other DC-DC or DC-AC converters with significant improvement of efficiency and/or transient response even though the modulator itself can be build with only few and cheap components.

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